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DESIGN AND IMPLEMENTATION OF SERIAL DIVIDER USING 180NM PROCESS TECHNOLOGY

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ABSTRACT

This paper presents an efficient 4-bit unsigned binary serial divider and its implementation using 180nm CMOS process technology. The layout design of the serial divider circuit is efficiently optimized in terms of area. The serial divider circuit provides a good compromise between area and performance in divider design. The serial divider is designed based on repeated one's complement binary subtraction algorithm. The implementation consists of several combinational and sequential components such as 4-bit ripple carry adder, 2:1 multiplexers, D flip-flops and 4-bit synchronous up counter. The circuit analysis is carried out in terms of performance parameters such as transistor count, propagation delay and power consumption. According to the estimations done, the transistor count, propagation delay and power consumption of the serial divider without parasitics was found to be 568, 5.13ns and 196.2µW respectively.The presence of parasitics due to metal layers in the layout design increase propagation delay to 86.42ns and power consumption to 206µW.

Keywords: Area, Cadence, Layout, Power consumption, Propagation Delay, Parasitics.

INTRODUCTION

Technology scaling of transistor feature size has provided a remarkable innovation in silicon industry for the last three decades. Designers are striving for small silicon area, higher speeds, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. Circuit realization for low power and low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. The advances in VLSI technology, more and more functionality complexity have been integrated into digital designs to better support target applications. With many applications requiring support for arithmetic units, complex arithmetic modules like multipliers and dividers are now being extensively used in design.

Of all the elemental operations, division is the most complicated operation and can consume the most resources (in either silicon, to implement the algorithm in hardware or in time, to implement the algorithm in software). Binary division operation is of immense importance in the field of engineering science. Inherently, division operation is a sequential type of operation, thereby it is more costly in terms of computational complexity and latency (propagation delay) compared with other mathematical operations.

It is of little surprise that, an efficient division algorithm can considerably improve the performance of the ALU component of any digital circuit. In other words, an efficient division algorithm is one of the main aims of a designer while implementing an ALU circuit. Many division algorithms have been presented such as division by means of repeated subtraction, division based on successive approximation of quotient and carry free division algorithm.

Binary divider can be categorized in two types, serial divider and parallel divider. The operation of division in serial divider is done by means of repeated subtraction. Suppose we want to divide 19 by 3. So we repeatedly subtract 3 from 19 and after six times subtraction, remainder is one, so less than divisor, so further subtraction is stopped. So the quotient comes out as six and the remainder is one. Binary division is done in the same way.

The proposed 4-bit binary serial divider is implemented using Cadence EDA tool [1]. The tool provides sophisticated features such as Cadence Virtuoso schematic editor which provides sophisticated capabilities which speed and ease the design, Cadence Virtuoso Visualization and Analysis which efficiently analyzes the performance of the design, Cadence Virtuoso Layout Suite that speeds up the physical layout of the design and Cadence Assura Physical Verification reduces overall verification time

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because it incorporates a fast and intuitive debug capability integrated within the Virtuoso custom design environment. It helps to easily recognize, fix, extract and compare errors.

THE PROPOSED SERIAL DIVIDER

The implementation of 4-bit unsigned binary serial divider [2] by means of repeated subtraction of two 4-bit unsigned binary numbers is shown in Fig.1. Here the divisor $Y_3Y_2Y_1Y_0$ is subtracted from $X_3X_2X_1X_0$ by one's complemented method of subtraction.

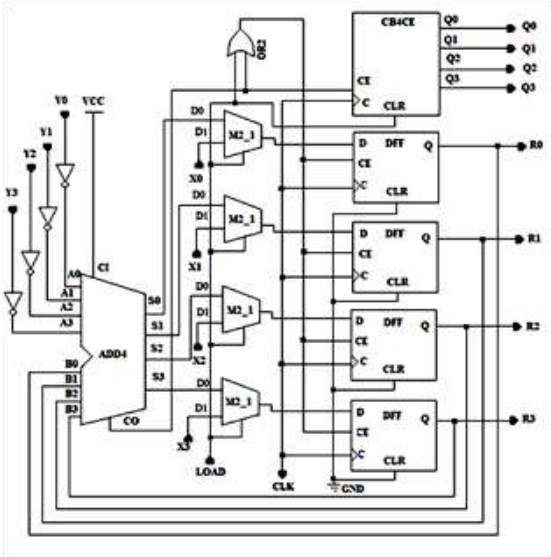

Fig.1 Implementation of serial divider

The basic building blocks used are

1) Adder (ADD4) to add two 4-bit binary numbers.
2) 4-bit binary synchronous up counter (CB4CE).
3) A set of four 2:1 MUX and
4) A set of four D flip-flops.

Each bit of divisor is complemented and fed to one set of adder inputs. Dividend is initially loaded in a register comprising of four D flip-flops by putting load input high, which is common select input of all the MUX and also to the CLR input of the counter. Initially, counter is also reset to zero. Output of the D flip-flops is fed to another set of inputs of adder. The final carry output (CO) of the adder block is fed into the clock enable input (CE) of the counter and also to an OR gate whose other input is LOAD and output goes to clock enable of register.

We assume that divisor (Y) and dividend (X) are non-zero numbers and X > Y, we shall have carry output of adder high initially since we are adding X with one's complement of Y. For one's complement method of subtraction there should be an end around carry. Here we are interested till there is a carry output in the adder and hence the carry input of the adder is tied high. So after the first clock we get X – Y at adder output which is stored in data register. The counter output is incremented to 0001.

In the next clock cycle we are subtracting Y from (X –Y), if (X –Y) > Y and counter output will increment to 0010. In the third clock cycle we are subtracting Y from (X- 2Y), if (X -2Y) > Y and counter output will increment to 0011. In this way subtraction continues till carry output of the adder is high. The register and counter are disabled when carry output of the adder is low and counting will be stopped. Thus the output of the counter ($Q_3Q_2Q_1Q_0$) is equal to the quotient and output from the data register is equal to the remainder ($R_3R_2R_1R_0$).

4-bit Ripple Carry Adder

Ripple carry adder is built using multiple full adders. The simple implementation of 4-bit ripple carry adder is shown in Fig.2. C_0 is the input carry, X_0 through X_3 and Y_0 through Y_3 represents two 4-bit input binary numbers.

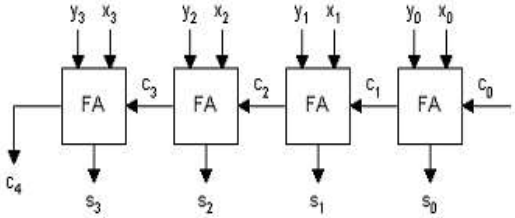

Fig.2 4-bit ripple carry adder

The full adder used in the divider is transmission gate full adder [3]. It uses a novel exclusive-or (XOR) gate. The schematic for this XOR gate is shown in Fig.3. The operation of the gate is explained as follows:

1) When signal A is high, -A is low. Transistor pair P1 and N1 thus acts as inverter, with –B appearing at the output. The transmission gate formed by transistor pair P2 and N2 is open.

2) When signal A is low, -A is high. The transmission gate formed by transistor pair P2 and N2 is now closed, passing B to the output. The inverter formed by transistor pair P1 and N1 is partially disabled.

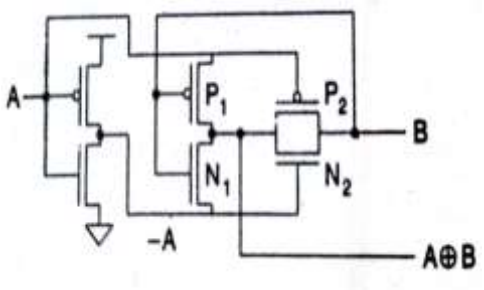

Fig. 3 Transmission gate XOR

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Thus this transistor configuration forms a 6-transistor XOR gate. By using four transmission gates, four inverters and two XOR gates, an adder may be constructed according to Fig.4. A xor B and the complement are formed using the transmission gate XOR gate shown in Fig.3. The Sum (A xor B xor Cin) is formed by a multiplexer controlled by A xor B (and complement). When A xor B is true, Cout = Cin and when A xor B is false, Cout = A (or B).

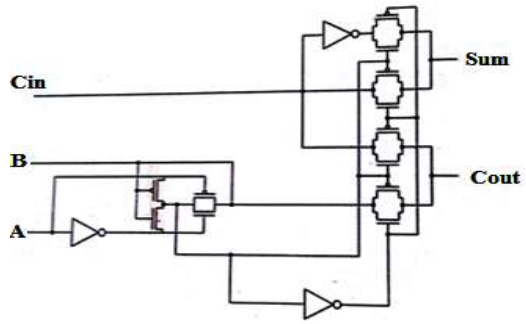

Fig. 4 Transmission gate Full Adder

2:1 Multiplexer

The multiplexer used in the divider design uses two transmission gates and an inverter as shown in the Fig.5.The transmission gates select input A or B on the basis of the value of the control signal S. When S=0, Y=A and when S=1, Y=B.

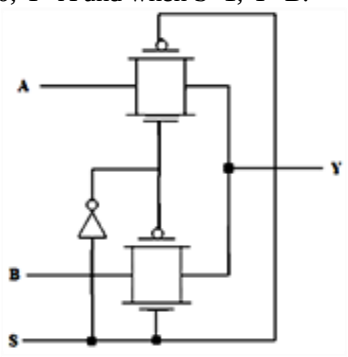

Fig. 5 Transmission gate 2:1 multiplexer

D Flip-flop

Fig.6 shows negative edge-triggered master-slave D flip-flop using D latches with enable input. It responds on the negative edge of the enable input (usually a clock). When the clock is high, the D input is stored in the first latch, but the second latch cannot change state. When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state. The result is that output can only change state when the clock makes a transition from high to low.

Master changes its state when clock is high while the latter changes its state when clock is low. When the clock is high the master tracks the value of D but since the slave is in inactive state, Qs also remains unchanged. When the clock signal goes low, the master goes to inactive state and the slave which is now in active state tracks the value of Qm. While clock is low, Qm does not change its value. Thus only once during the clock cycle the slave can undergo change in its value. It can also be observed that only during the transition from high to low, the output gets change.

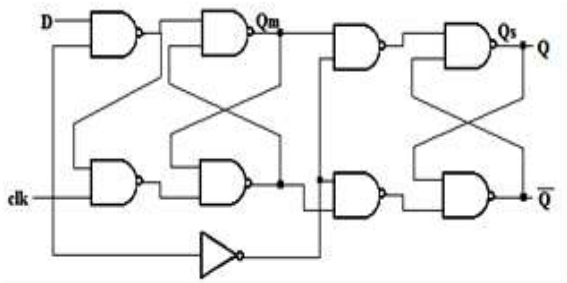

Fig. 6 Negative edge-triggered master-slave D flip-flop

Fig.7 shows the implementation of master-slave D flip-flop with clear (clr) and enable (CE) inputs. When the clear input goes high, irrespective of the inputs D and enable, the output goes low. When the enable input goes low, irrespective of the inputs D and clear, the output follows the previous state.

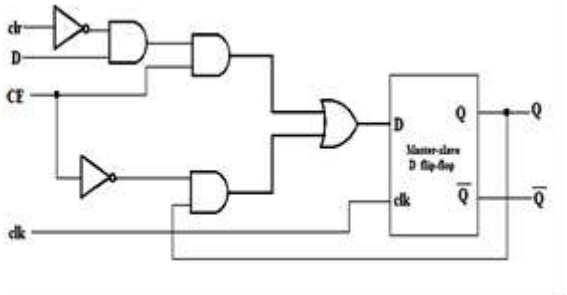

Fig. 7 Master-slave D flip-flop with clr and CE inputs

Counter

The synchronous 4-bit up counter has 3 AND gates, 4 XOR gates and 4 master-slave D flip-flops. Same clock pulse is given to each flip-flop. So with every clock pulse the counter counts one step up. It is an up counter and starts from 0000. Then with clock pulse counts like 0001, 0010, 0011, 0100 up to 1111. Then it starts from 0000 again. Q0 is the LSB and Q3 is the MSB. The master-slave D flip-flop actually works at the falling edge of the clock [4]. But because it is a master-slave configuration, it actually stores the input at rising edge and it is given to the output at the falling edge of the clock. So change in counter output is observed in the falling edge of the clock.

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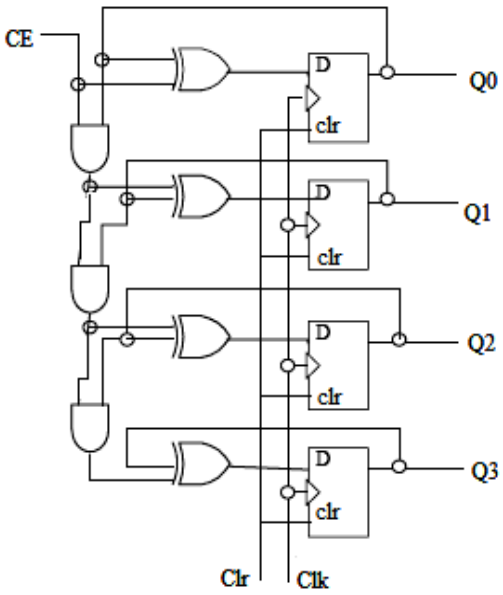

Fig. 8 Synchronous 4-bit up counter

SCHEMATIC AND LAYOUT

The proposed serial divider is implemented in Cadence EDA tool [1]. The transistor level diagram is implemented using Cadence Virtuoso schematic editor. The optimized layout is designed using Cadence Virtuoso Layout Suite. The implementation of the 4-bit serial divider will be performed progressively by implementing and creating instances of the components of the counter independently and subsequently using all the components together to create the divider circuit.

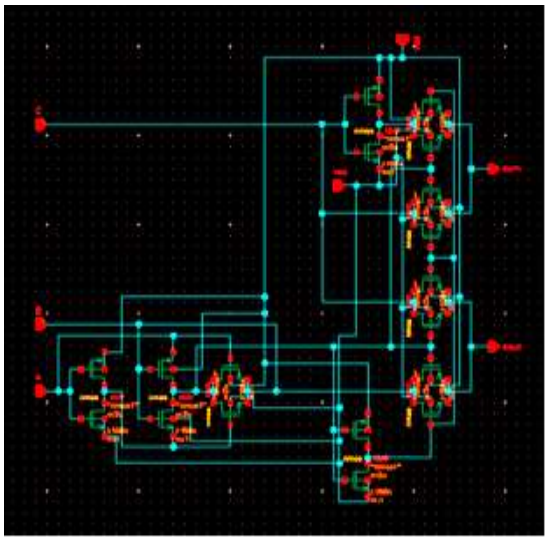

Fig. 9 Schematic of transmission gate full adder

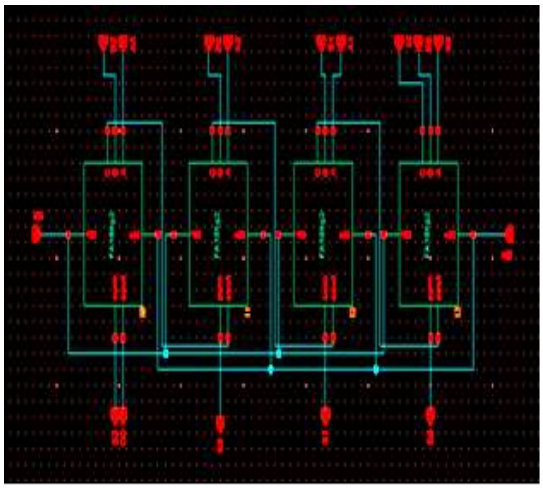

Fig. 10 Schematic of 4-bit ripple carry adder

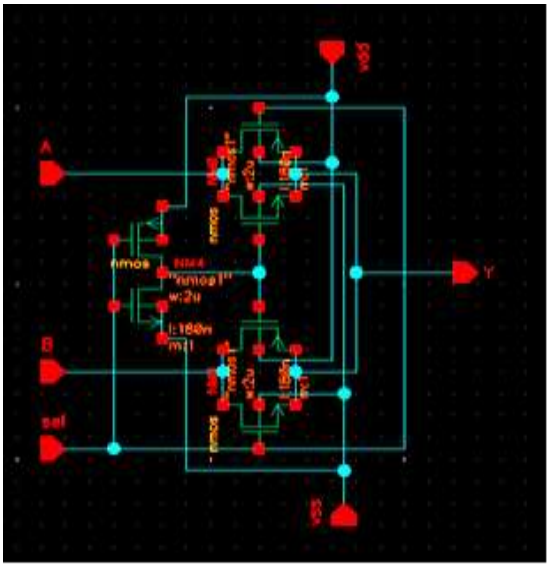

Fig. 11 Schematic of 2:1 multiplexer

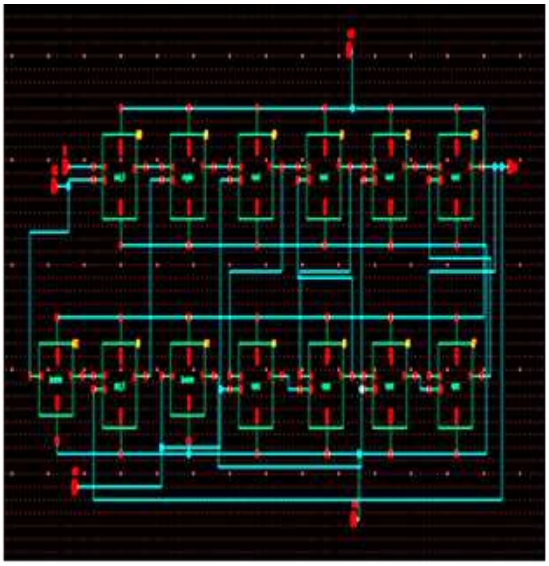

Fig. 12 Schematic of D flip-flop

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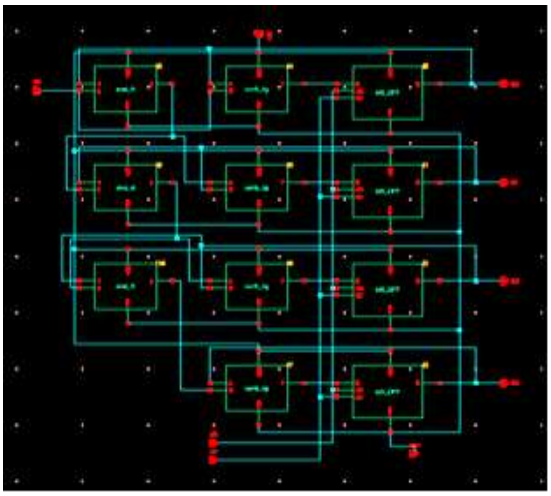

Fig.13 Schematic of counter

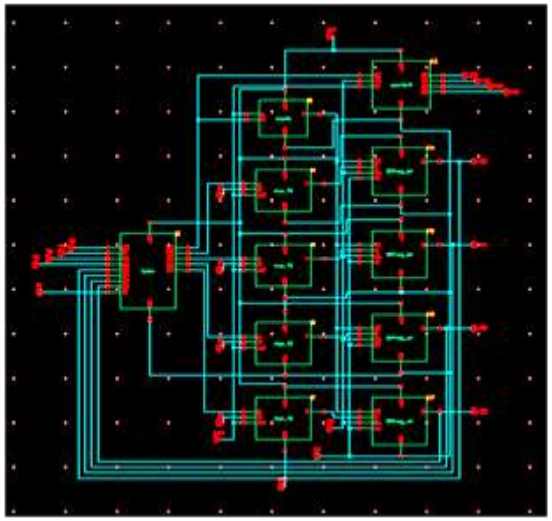

Fig.14 Schematic of serial divider

The optimized layouts of all the blocks of divider circuit are designed using sea of gate arrays concept in order to reduce the area. All the layouts are designed following the design rules of 180nm CMOS process technology.

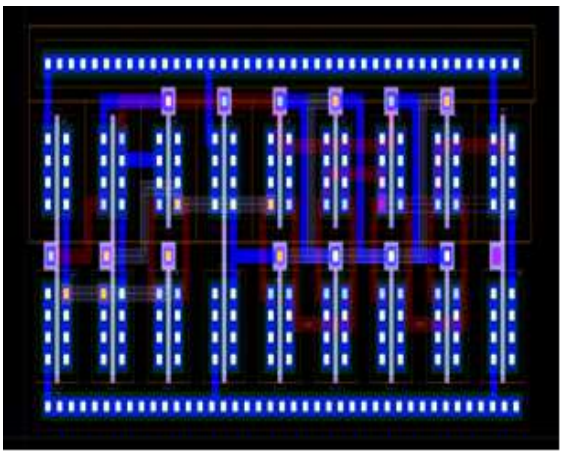

Fig. 15 Layout of transmission gate full adder

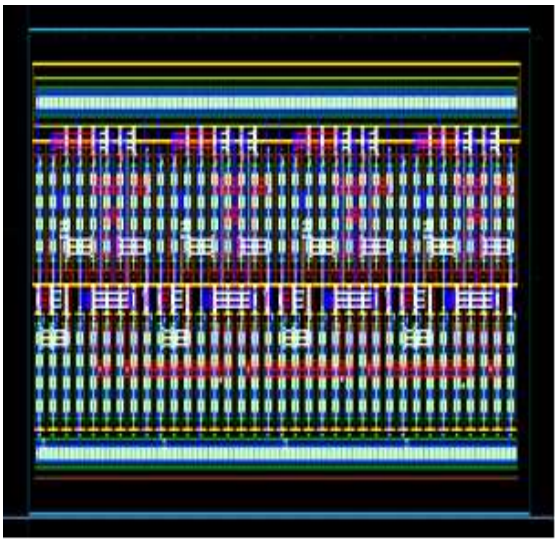

Fig. 16 Layout of 4-bit ripple carry adder

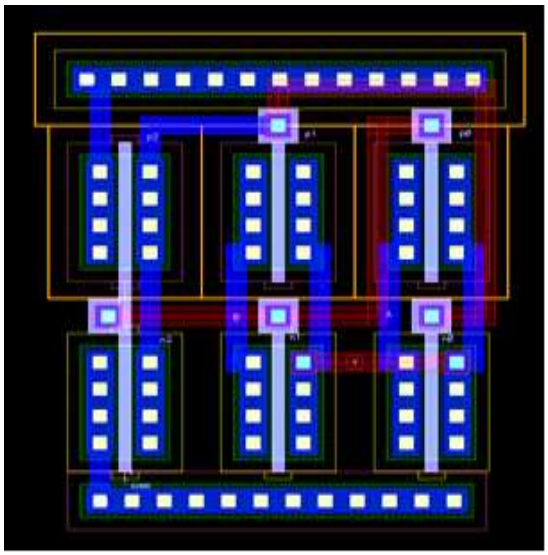

Fig.17 Layout of 2:1 multiplexer

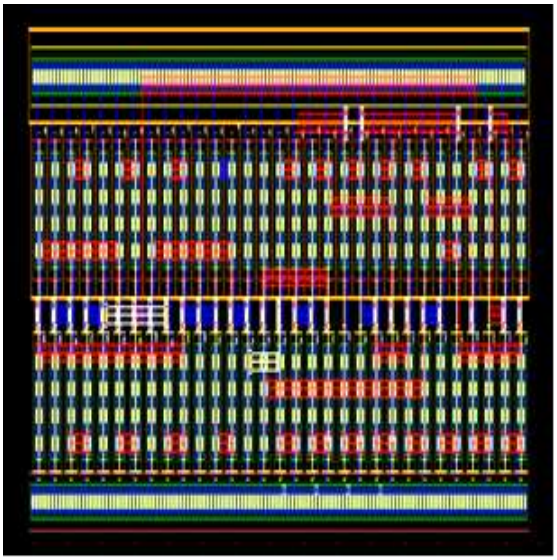

Fig. 18 Layout of D flip-flop

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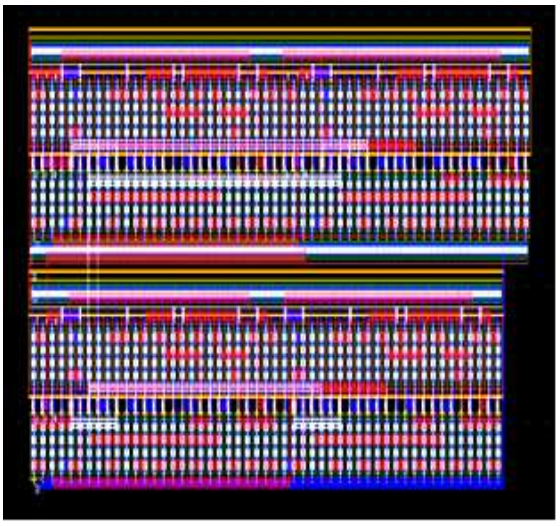

Fig. 19 Layout of counter

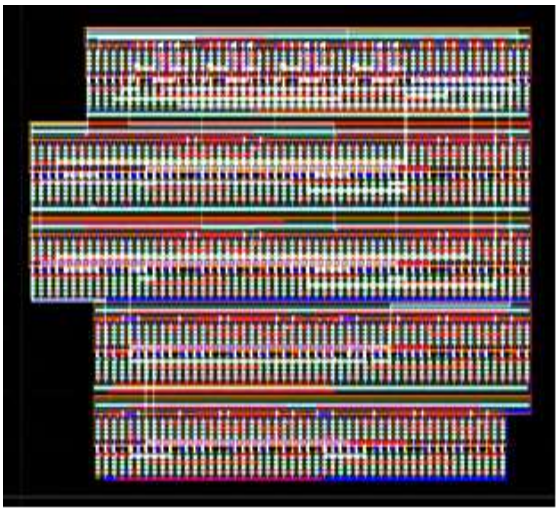

Fig. 20 Layout of serial divider

SIMULATION RESULTS

The layouts of all the individual blocks and the final divider circuit are simulated and the transient responses are analyzed using Cadence analog design environment.

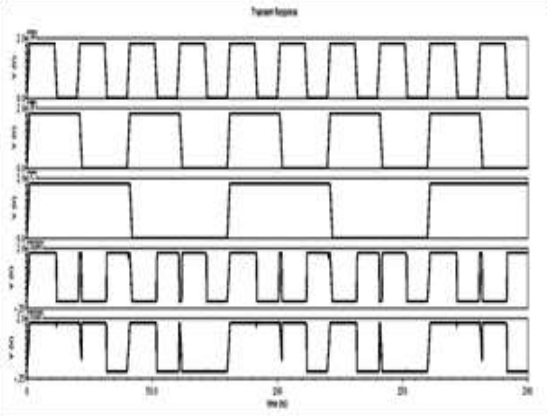

Fig. 21 Transient response of transmission gate full adder

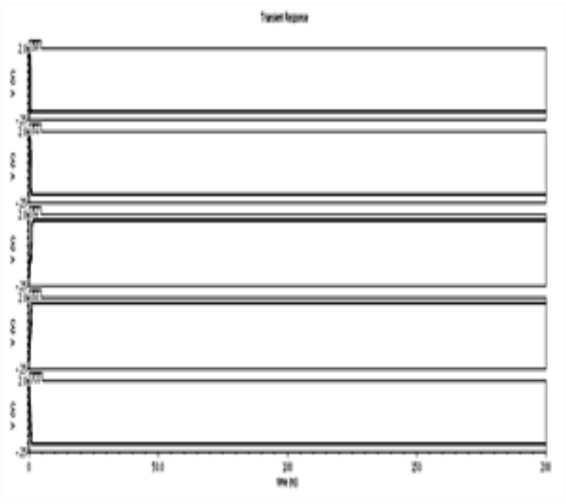

Fig. 22 Transient response of 4-bit adder with A=0101, B=0110, Cin=1

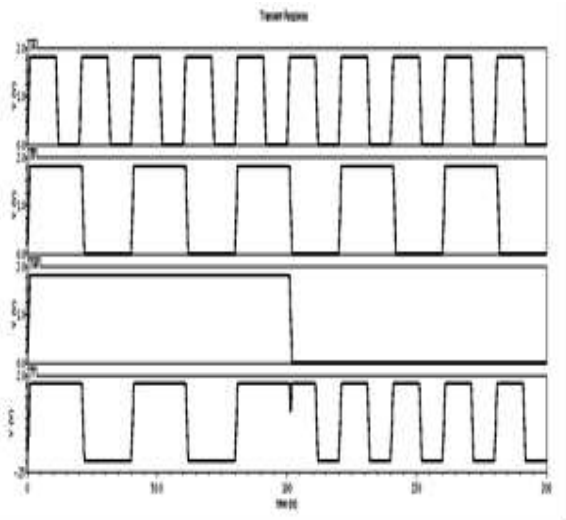

Fig. 23 Transient response of 2:1 multiplexer

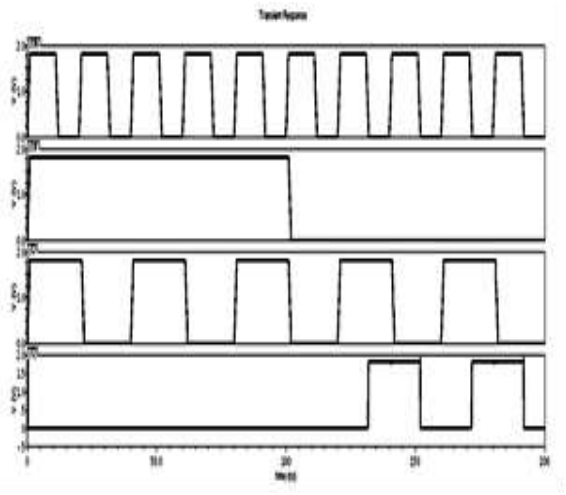

Fig. 24 Transient response of D flip-flop

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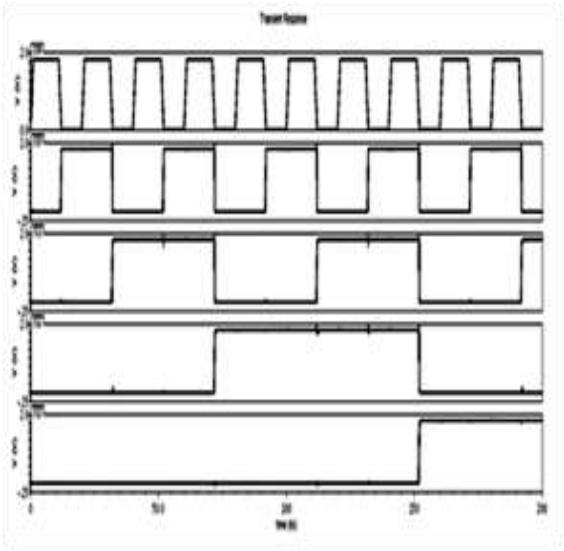

Fig. 25 Transient response of counter

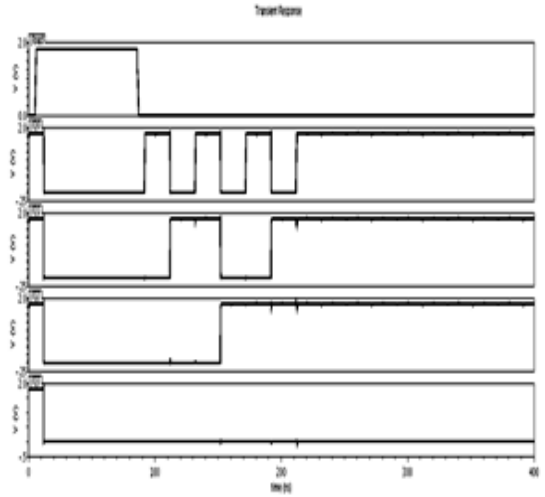

Fig. 26 (a)

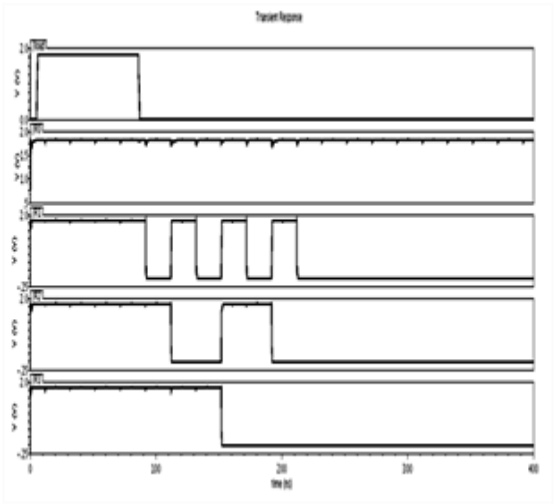

Fig. 26 (b)

Fig. 26 Transient response of serial divider without parasitics X=1111, Y=0010 (a) Quotient; (b) Remainder

The existence of parasitic components creates distortion in the waveforms during the high-to-low or low-to-high transitions of the input signals. This creates kink (distortion) in the output signals during the transitions and increases propagation delay and power consumption. The simulation of divider circuit with parasitics is shown in Fig.27.

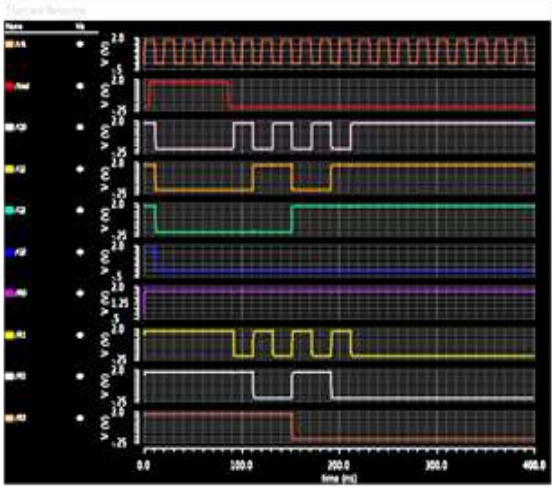

Fig. 27 Transient response of serial divider with parasitics X=1111, Y=0010

The serial divider circuit and all its individual blocks: 4-bit ripple carry adder, 2:1 multiplexer, D flip-flop and synchronous 4-bit up counter are analyzed in terms of transistor count, propagation delay and power consumption. The divider circuit is individually analyzed for the same parameters with and without the effect of parasitics.

Table 1. Performance analysis of each block of serial divider

Circuits	Transistor count	Delay	Power
Transmission gate FA	18	21.02ns	22.01µW
4-bit RCA	72	22.47ps	3.52µW
2:1 MUX	6	21.02ns	667.80µW
D flip-flop	62	71.38ns	36.22µW
Counter	210	211.40ns	97.90µW

Table 2. Performance analysis of serial divider

Serial Divider	Transistor count	Delay	Power
Without parasitics	568	5.13ns	196.20µW
With parasitics	568	86.42ns	206µW

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CONCLUSION

In this project, we presented design and implementation of 4-bit unsigned binary serial divider based on repeated 1's complement subtraction of binary numbers. The divider is implemented in Cadence EDA tool as well as Xilinx ISE tool. The simulation results match the expected results with accuracy. The main aim to optimize the divider design in terms of area has been achieved successively. The performance of the divider circuit is analyzed in terms of parameters such as transistor count, propagation delay and power consumption. According to the estimations carried out, we found that the presence of parasitics due to various metal layers used in the layout design resulted in the output distortion during high-to-low and low-to-high transitions. Subsequently there is an increase in the propagation delay and power consumption. The estimation comparisons between the serial divider layout without and with parasitics show that there is 81.29 ns increase in the delay and 9.8µW increase in the power consumed.

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